ENC28J60

ENC28J60 Silicon Errata and Data Sheet Clarification

The ENC28J60 devices that you have received conform functionally to the current Device Data Sheet (DS39662**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon listed in Table 1. The silicon issues are summarized in Table 2. Issues specific to technical conformance with IEEE Std. 802.3 are listed in Table 3.

Data Sheet clarifications and corrections start on page 9, following the discussion of silicon issues.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 and Table 3 apply to the current silicon revision (**B7**).

The silicon revision level can be retrieved by querying the read-only EREVID register, located at address 12h in Bank 3 of the device's Control register space. Please refer to the Device Data Sheet for detailed information on accessing this register. The values for the various ENC28J60 silicon revisions are shown in Table 1.

TABLE 1: SILICON EREVID VALUES

Part Number	B1	B4	B5	B7
ENC28J60	0000 0010	0000 0100	0000 0101	0000 0110

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Issue	Issue Summary	Affected Revisions			
				B1	B4	B5	B7
MAC Interface	—	1.	MAC registers unreliable with slow asynchronous SPI clock	X	X		
Reset	—	2.	CLKRDY set early	X	X	X	X
Core	Operating Specifications	3.	Industrial (-40°C to +85°C) temperature range unsupported	X	X		
Oscillator	CLKOUT pin	4.	CLKOUT unavailable in Power Save mode	X	X	X	X
Memory	Ethernet Buffer	5.	Receive buffer must start at 0000h	X	X	X	X
Interrupts	—	6.	Receive Packet Pending Interrupt Flag (PKTIF) unreliable	X	X	X	X
PHY	—	7.	TPIN+/- automatic polarity detection and correction unreliable	X	X	X	X
PHY	—	8.	RBIAS resistor value differs between silicon revisions	X	X		
PHY	—	9.	Internal loopback in half-duplex unreliable	X	X	X	X
PHY	—	10.	Internal loopback in full-duplex unreliable	X	X	X	X
PHY LEDs	—	11.	Combined Collision and Duplex Status mode unavailable	X	X	X	X
Transmit Logic	—	12.	Transmit abort may stall transmit logic	X	X	X	X
PHY	—	13.	Received link pulses potentially cause collisions			X	X
Memory	Ethernet Buffer	14.	Even values in ERXRDPT may corrupt receive buffer	X	X	X	X
Transmit Logic	—	15.	LATECOL Status bit unreliable	X	X	X	X
PHY LEDs	—	16.	LED auto-polarity detection unreliable	X	X	X	X
DMA	—	17.	DMA checksum calculations will abort receive packets	X	X	X	X
Receive Filter	—	18.	Pattern match filter allows reception of extra packets	X	X	X	X
SPI Interface	—	19.	Reset command unavailable in Power Save mode	X	X	X	X

TABLE 3: ETHERNET CONFORMANCE ISSUES

Issue	Issue Summary	Affected Revisions			
		B1	B4	B5	B7
1.	TP_IDL transmit waveform violates IEEE STD 802.3™ template	X	X		
2.	PHY accepts receive packet in Link Test Fail state	X	X		
3.	Collision enforcement is delayed	X	X		

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B7**).

1. Module: MAC Interface

When the SPI clock from the host microcontroller is run at frequencies of less than 8 MHz, reading or writing to the MAC registers may be unreliable.

Work around

Two work arounds are presented; others may be available.

1. Run the SPI at frequencies of at least 8 MHz.
2. Generate an SPI clock of 25/2 (12.5 MHz), 25/3 (8.333 MHz), 25/4 (6.25 MHz), 25/5 (5 MHz), etc., and synchronize with the 25 MHz clock entering OSC1 on the ENC28J60. This could potentially be accomplished by feeding the same 25 MHz clock into the ENC28J60 and host controller. Alternatively, the host controller could potentially be clocked off of the CLKOUT output of the ENC28J60.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X						

2. Module: Reset

After sending an SPI Reset command, the PHY clock is stopped but the ESTAT.CLKRDY bit is not cleared. Therefore, polling the CLKRDY bit will not work to detect if the PHY is ready.

Additionally, the hardware start-up time of 300 μs may expire before the device is ready to operate.

Work around

After issuing the Reset command, wait at least 1 ms in firmware for the device to be ready.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

3. Module: Core (Operating Specifications)

The device data sheet specifies that industrial operating temperature range (-40°C to +85°C) is supported. However, silicon revisions B1 and B4 only support the commercial temperature range (0°C to +70°C).

Work around

Use silicon revision B5 or later.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X						

4. Module: Oscillator (CLKOUT Pin)

No output is available on CLKOUT while operating in Power Save mode (ECON2.PWRSV = 0).

Work around

If the host controller uses the CLKOUT signal as the system clock, do not enable Power Save mode.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

5. Module: Memory (Ethernet Buffer)

The receive hardware maintains an internal Write Pointer which defines the area in the receive buffer where bytes arriving over the Ethernet are written. This internal Write Pointer should be updated with the value stored in ERXST whenever the Receive Buffer Start Pointer, ERXST, or the Receive Buffer End Pointer, ERXND, is written to by the host microcontroller. Sometimes, when ERXST or ERXND is written to, the exact value, 0000h, is stored in the internal receive Write Pointer instead of the ERXST address.

Work around

Use the lower segment of the buffer memory for the receive buffer, starting at address 0000h. For example, use the range (0000h to n) for the receive buffer and ((n + 1) to 8191) for the transmit buffer.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

6. Module: Interrupts

The Receive Packet Pending Interrupt Flag (EIR.PKTIF) does not reliably/accurately report the status of pending packets.

Work around

In the Interrupt Service Routine (ISR), if it is unknown if a packet is pending and the source of the interrupt, switch to Bank 1 and check the value in EPKTCNT.

If polling to see if a packet is pending, check the value in EPKTCNT.

Note: This errata applies only to the interrupt flag. If the receive packet pending interrupt is enabled, the $\overline{INT}$ pin will continue to reliably become asserted when a packet arrives. The receive packet pending interrupt is cleared in the same manner described in the data sheet.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

7. Module: PHY

The automatic RX polarity detection and correction features of the PHY layer do not work as described. When incorrect RX polarity is present, poor receive network performance, or no receive activity with some link partners, may occur.

Work around

When designing the application, always verify that the TPIN+ and TPIN- pins are connected correctly.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

8. Module: PHY

The external resistor value recommended for RBIAS in the current revision of the data sheet does not apply to certain revisions of silicon. Using an incorrect resistor value will cause the Ethernet transmit waveform to violate IEEE 802.3 specification requirements.

Work around

For silicon revisions, B1 and B4, use a 2.7 kΩ, 1% external resistor between the RBIAS pin and ground. The value shown in the data sheet (2.32 kΩ,) is correct for revisions B5 and B7.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X						

9. Module: PHY

The PHY Half-Duplex Loopback mode, enabled when PHCON1.PDPXMD = 0, PHCON2.HDLDIS = 0 and PHCON2.FRCLNK = 1, or a link partner is connected, does not loop packets back to itself reliably.

Work around

Perform loopback diagnostics in full duplex using an external loopback connector/cable. To avoid looping occasional packets back to one self, PHCON2.HDLDIS should be set by the host controller. PHCON2.HDLDIS is clear by default.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

10. Module: PHY

The PHY Full-Duplex Loopback mode, enabled when PHCON1.PDPXMD = 1 and PHCON1.PLOOPBK = 1, does not loop packets back to itself reliably.

Work around

Perform loopback diagnostics in full duplex using an external loopback connector/cable.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

11. Module: PHY LEDs

When the PHLCON register is programmed to output the duplex status and collision activity on the same LED (‘1110’), only the duplex status will be displayed (i.e., the LED will be illuminated when in Full-Duplex mode and extinguished when in Half-Duplex mode, regardless of collision activity).

Work around

When Half-Duplex mode is being used, program the PHLCON register’s LxCFG bits with ‘0011’ to display the collision status. When Full-Duplex mode is being used, program the PHLCON register’s LxCFG bits with ‘0101’ to display the duplex status.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

12. Module: Transmit Logic

In Half-Duplex mode, a hardware transmission abort caused by excessive collisions, a late collision or excessive deferrals, may stall the internal transmit logic. The next packet transmit initiated by the host controller may never succeed (ECON1.TXRTS will remain set indefinitely).

Work around

Before attempting to transmit a packet (setting ECON1.TXRTS), reset the internal transmit logic by setting ECON1.TXRST and then clearing ECON1.TXRST. The host controller may wish to issue this Reset before any packet is transmitted (for simplicity), or it may wish to conditionally reset the internal transmit logic based on the Transmit Error Interrupt Flag (EIR.TXERIF), which will become set whenever a transmit abort occurs. Clearing ECON1.TXRST may cause a new transmit error interrupt event (EIR.TXERIF will become set). Therefore, the interrupt flag should be cleared after the Reset is completed.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

13. Module: PHY

When transmitting in Half-Duplex mode with some link partners, the PHY will sometimes incorrectly interpret a received link pulse as a collision event. If less than, or equal to, MACLCON2 bytes have been transmitted when the false collision occurs, the MAC will abort the current transmission, wait a random back-off delay and then automatically attempt to retransmit the packet from the beginning – as it would for a genuine collision.

If greater than MACLCON2 bytes have been transmitted when the false collision occurs, the event will be considered a late collision by the MAC and the packet will be aborted without retrying. This causes the packet to not be delivered to the remote node. In some cases, the abort will fail to reset the transmit state machine.

Work around

Implement a software retransmit mechanism whenever a late collision occurs.

When a late collision occurs, the associated bit in the transmit status vector will be set. Also, the EIR.TXERIF bit will become set, and if enabled, the transmit error interrupt will occur.

If the transmit state machine does not get reset, the ECON1.TXRTS bit will remain set and no transmit interrupt will occur (the EIR.TXIF bit will remain clear).

As a result, software should detect the completion of a transmit attempt by checking both TXIF and TXERIF. If the Transmit Interrupt (TXIF) did not occur, software must clear the ECON1.TXRTS bit to force the transmit state machine into the correct state.

The logic in Example 1 (following page) will accomplish a transmission and any necessary retransmissions with a maximum retry abort.

Affected Silicon Revisions

B1	B4	B5	B7				
		X	X				

EXAMPLE 1:

```
ECON1.TXRST  = 1
ECON1.TXRST  = 0
EIR.TXERIF   = 0
EIR.TXIF     = 0
ECON1.TXRTS  = 1
while(EIR.TXIF = 0 and EIR.TXERIF = 0)
       NOP
ECON1.TXRTS    = 0
read tsv
for retrycount = 0 to 15
    if (EIR.TXERIF and tsv<Transmit Late Collision>) then
        ECON1.TXRST  = 1
        ECON1.TXRST  = 0
        EIR.TXERIF   = 0
        EIR.TXIF     = 0
        ECON1.TXRTS  = 1
        while(EIR.TXIF = 0 and EIR.TXERIF = 0)
               NOP
        ECON1.TXRTS  = 0
        read tsv
    else
        exit for
    end if
next retrycount
```

14. Module: Memory (Ethernet Buffer)

The receive hardware may corrupt the circular receive buffer (including the Next Packet Pointer and receive status vector fields) when an even value is programmed into the ERXRDPTH:ERXRDPTL registers.

Work around

Ensure that only odd addresses are written to the ERXRDPT registers. Assuming that ERXND contains an odd value, many applications can derive a suitable value to write to ERXRDPT by subtracting one from the Next Packet Pointer (a value always ensured to be even because of hardware padding) and then compensating for a potential ERXST to ERXND wrap-around. Assuming that the receive buffer area does not span the 1FFFh to 0000h memory boundary, the logic in Example 2 will ensure that ERXRDPT is programmed with an odd value:

EXAMPLE 2:

```
if (Next Packet Pointer = ERXST)
    then:
ERXRDPT = ERXND
    else:
ERXRDPT = Next Packet Pointer – 1
```

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

15. Module: Transmit Logic

If a collision occurs after 64 bytes have been transmitted, the transmit logic may not set the Late Collision Error status bit (ESTAT.LATECOL).

Work around

Whenever a late collision has potentially occurred (both EIR.TXERIF and ESTAT.TXABRT bits will be set), read the transmit status vector and check the transmit late collision bit (bit 29).

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

16. Module: PHY LEDs

With some LEDs, the LED auto-polarity detection circuit misdetects the connected polarity of the LED upon Reset. As a result, the LED output pin will sink current when it should be sourcing current and vice versa. The LED will visually appear inverted. For example, an LED configured to display the link status will be illuminated when no link is present and extinguished when a link has been established. The likelihood of a misdetection will vary over temperature. If LEDB is misdetected, the PHCON1.PDPXMD bit will also reset to the incorrect state.

Work around

Place a resistor in parallel with the LED. The resistor value needed is not critical. Resistors between 1 kΩ and 100 kΩ are recommended.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

17. Module: DMA

If the DMA module is operated in Checksum mode (ECON1.CSUMEN, DMAST = 1) at any time while a packet is currently being received from the Ethernet (ESTAT.RXBUSY = 1), the packet being received will be aborted. The packet abort will cause the Receive Error Interrupt Flag (EIR.RXERIF) to be set, the interrupt will occur, if enabled, and the Buffer Error status bit (ESTAT.BUFER) will also become set. The packet will be permanently lost.

Work around

Do not use the DMA module to perform checksum calculations; perform checksums in software. This problem does not affect the DMA copy operation (ECON1.CSUMEN = 0).

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

18. Module: Receive Filter

If using the Pattern Match receive filter, some packets may be accepted that should be rejected. Specifically, if ERXFCON.ANDOR = 0, ERXFCON.PMEN = 1 and at least one of the Hash Table, Magic Packet™, Broadcast, Multicast or Unicast receive filters are enabled, then packets can be accepted that do not meet any of the enabled filter criteria. This will occur if the receive packet is less than or equal to 64+EPMO bytes long. For typical applications using the Pattern Match and Unicast receive filters simultaneously with a zero Pattern Match offset, this will result in the reception of unwanted 64-byte Address Resolution Protocol (ARP) broadcast frames, among possible others.

Work around

When using the pattern match receive filter, discard any unwanted packets in software.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

19. Module: SPI Interface

When operating in Power Save mode (ECON2.PWRSV = 1), issuing the SPI System Reset command will have no effect.

Work around

Clear the PWRSV bit and wait for the device's power regulator to stabilize before issuing an SPI System Reset command.

For a device in an unknown state, the recommended Reset sequence is:

1. Use the Bit Field Clear command and clear ECON2.PWRSV (ECON2<5>).
2. Wait at least 300 µs for power to be restored.
3. Issue the System Reset command.
4. Wait 1 ms for the Reset to complete and to ensure that all modules are ready to be used.
5. Confirm that the Reset has taken place. This can be accomplished by reading a register and checking for an expected Reset value. For example, read ESTAT and confirm that the CLKRDY bit (bit 0) is set and the unimplemented bit (bit 3) is clear.
   If one or both of these conditions are not met, this may indicate that the ENC28J60 is not ready yet (e.g., the microcontroller has exited POR while ENC28J60 is still powering up). In this case, repeat the procedure from Step 1.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X	X	X				

Ethernet Conformance Issues

The following conformance issues were noted in testing the B1 and B4 silicon revisions for compliance with IEEE Standard 802.3. These issues are not present after Revision B4 and are included for informational purposes.

1. Issue: TP_IDL Pattern

The observed TP_IDL pattern transmitted by ENC28J60 was observed to not stay within the standard defined template when using the TPM (Twisted Pair Model) and TP Test Load 2.

Reference: IEEE Std 802.3, §14.3.1.2.1, Figures 14-10 and 14-11

Potential Application Impact

The TP_IDL test requires a total of six separate subtests, using three different test loads with and without TPM. The fact that the device consistently passed five of the six sub tests, while narrowly missing the sixth, leads to the conclusion that this is a minor issue. No failures have been observed due to this issue.

Work around

Use silicon revision B5 or later.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X						

2. Issue: Exiting Link Test Fail State

The ENC28J60 was observed to improperly accept a frame with no preceding LTPs (Link Test Pulse). When a device is in the Link Test Fail state, it should exit this state when a valid packet is received, however, the first packet should not be accepted. The second and subsequent packets should be accepted while the device is in the Link Test Pass state.

Reference: IEEE Std 802.3, Figure 14-6

Potential Application Impact

Link Test Pulse is an integral part of every 10Base-T system. It is used to notify a link partner of the presence of a 10Base-T device. An absence of LTPs signifies that the Ethernet cable is not connected or a link partner is missing. Even when a cable is not connected, a 10Base-T device would continuously send out LTPs. This fact makes it unlikely that there will ever be a situation in which a device would be receiving valid Ethernet frames without already being in the Link Test Pass state. In the unlikely event that this situation does occur, higher layer protocols would protect the system from accepting unwanted data. It is unlikely that this failure will have significant impact on a networked application. No failures have been observed due to this issue.

Work around

Use silicon revision B5 or later.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X						

3. Issue: Collision Handling

The delay from the collision event to collision enforcement with the jam pattern is approximately 50 BT (Bit Times), which is greater than the specified limit of 36 BT.

Reference: IEEE Std 802.3, Annex B, § B.1.2

Potential Application Impact

A collision in a half-duplex 10Base-T is not an unexpected event. It exists as a normal part of the network operation. The purpose of the jam pattern is to ensure that the duration of the collision is sufficient to be noticed by the other transmitting station(s) involved in the collision. A longer delay between the collision event and the start of jam pattern would cause the duration of the collision to be longer.

After each collision, both transmitting stations would back off and wait a random amount of time before attempting to transmit again. The minimum Idle time between each Ethernet frame is 9.6 μs. The longer collision duration of 14 BT, or 1.4 μs, can be considered as a small fraction of time wasted for each collision. It is unlikely that this issue will have significant impact on networked applications. No failures have been observed due to this issue.

Work around

Use silicon revision B5 or later.

Affected Silicon Revisions

B1	B4	B5	B7				
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39662**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Receive Filter

In **Section 8.2 "Pattern Match Filter"**, it is stated that the pattern match offset programmed into the EPMOH:EPMOL registers should be loaded with the offset from the beginning of the destination address field. This implies that any value can be used. In fact, for correct operation, it is required that the EPMOH:EPMOL registers be programmed with an even value only (i.e., EPMOL<0> must always be '0').

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2007)

Original revision. Silicon errata issues 1 (Reset), 2 (Oscillator – CLKOUT Pin), 3 (Memory – Ethernet Buffer), 4 (Interrupts), 5-8 (PHY), 9 (PHY LEDs), 10 (Transmit Logic), 11 (Memory – Ethernet Buffer), 12 (Transmit Logic), 13-14 (PHY) and 15 (DMA).

Rev B Document (07/2008)

Updated the revision of the referenced data sheet. Changed the revision identifier for this device as the previous version contained an error.

Rev C Document (07/2010)

Revises the document to include all released silicon revisions of the device, starting with revision B1, and removes “silicon revision B7” from the title. Order of issues has been re-aligned to better reflect sequential issue history:

- 1 (MAC Interface)
- 2 (Reset)
- 3 (Core)
- 4 (Oscillator)
- 5 (Memory)
- 6 (Interrupts)
- 7-10 (PHY)
- 11 (PHY LEDs)
- 12 (Transmit Logic)
- 13 (PHY)
- 14 (Memory – Ethernet Buffer)
- 15 (Transmit Logic)
- 16 (PHY)
- 17 (DMA)

Adds new silicon issues 18 (Receive Filter) and 19 (SPI Interface) to all silicon revisions.

Makes minor clarifying changes and typographic corrections to issues 2, 3, 4, 5, 7, 13 and 14.

Revises issue 8 (PHY) to reflect that the current revision of the data sheet correctly describes the current silicon revision.

Adds Ethernet Conformance Issues 1 (TP_IDL Pattern), 2 (Exiting Link Test Fail State) and 3 (Collision Handling) from previous revisions B1 and B4.

Adds Data Sheet Clarification 1 (Receive Filters).

This document replaces these errata documents:

- DS80254, *“ENC28J60 Revision B1 Silicon Errata”*
- DS80257, *“ENC28J60 Revision B4 Silicon Errata”*
- DS80264, *“ENC28J60 Revision B5 Silicon Errata”*

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